REMARKS

In the Official Action, all pending claims 1-12 were rejected by the Examiner. While Applicants respectfully traverse the rejections, Applicants have amended claim 1. Reconsideration of the application in view of the remarks and amendments set forth below is respectfully requested.

Rejection Under 35 U.S.C. § 102

The Examiner rejected claims 1-6 and 8-11 under 35 U.S.C. § 102(b) as being anticipated by McAdams (U.S. Pat. No. 5,301,160). Specifically, the Examiner stated:

> Regarding **claim 1**, McAdams discloses a system comprising: a processor (fig. 1, 102), a power supply coupled to the processor (fig. 1, 112); and a device coupled to the processor and the power supply and comprising (fig. 2): an internal power supply bus configured to receive a power signal from the power supply (fig. 2, buses internal to 145 supplying Vdd 112); and an isolation circuit configured to disconnect the internal power supply bus from the power supply bus by interrupting the flow of the power signal (fig. 2, isolating circuit being p-mos transistors 282 and 284, which are configured to interrupt the power signals to TL and TR lines, which feed powers to the memory section, right dotted box in fig. 2).

Although Applicants have amended claim 1, Applicants respectfully assert that the McAdams reference does not anticipate the claimed subject matter. Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every

element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

The present application is directed to a technique for implementing a zero power standby mode with reduced leakage current. In operating electronic devices, a standby mode or a sleep state is typically implemented to maintain power to certain components when the system is not in use. Typical electronic devices lose some leakage current even though they are in a standby mode or a sleep state. *See* Application, p. 3, lines 15-22. To prevent or further reduce the leakage currents in the standby mode, an isolation circuit in accordance with the present invention may be implemented. *See* Application, p. 6, line 21-p. 7, line 3. The isolation circuit, which may be activated by a control signal, may be used to disconnect an internal power supply bus from an external voltage source to reduce leakage currents in response to initiating a standby mode. *See* Application, p. 9, lines 3-9, lines 15-27, p. 10, line 25-p. 11, line 7. Specifically, claim 1 recites "an isolation circuit configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit."

In contrast, the McAdams reference discloses a selection circuit that enables transmissions through transfer gates in response to address signals. *See* McAdams, col. 2, lines 31-32. The selection circuit provides either a pre-charged voltage to the transfer gates or a high level signal to one of the transfer gates when selecting a transfer gate. *See* McAdams, col. 2, lines 33-36. Specifically, the bitline isolation control circuit 145 includes two voltage supply

selection circuits that are controlled by signals produced from the row address decoder 124. *See* McAdams, col. 5, lines 15-17. The bitline isolation control circuit 145 switches between a pre-charged state and an active state depending on the row address select signals RA8 and $\overline{RA8}$ along with the row address selection signals RA9 and $\overline{RA9}$, which are applied to the inputs of the bitline isolation control circuit 145. *See* McAdams, col. 5, lines 26-47.

Applicants respectfully assert that the McAdams reference does not disclose "an isolation circuit configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit," as recited in claim 1. In the rejection of claim 1, the Examiner asserted that the bitline isolation control circuit 145 is equivalent to the "device" and that the enhancement mode MOS transistors 282 and 284 are equivalent to the "isolation circuit." Applicants also assume that the Examiner is asserting that the transfer control leads TR and TL are equivalent to the "internal power supply bus." However, Applicants respectfully assert that at best, the McAdams reference describes that row address select and selection signals RA8, RA9, $\overline{RA8}$ and $\overline{RA9}$ are used by the bitline isolation circuit 145 to select between two voltage supplies that are supplied to the transfer control leads TR and TL. *See* McAdams, col. 5, lines 26-32. In fact, the McAdams reference specifically describes that the voltage supply selection circuits are controlled by the signals produced from the row address decoder 124. *See* McAdams, col. 5, lines 15-17. These row address select and selection signals RA8, RA9, $\overline{RA8}$ and $\overline{RA9}$ are provided to the bit line isolation control circuit 145 to couple specific memory bitlines to the sense amplifier 200 through the transfer control leads TR and TL. *See* McAdams, col. 5, lines

21-32. Because the enhancement mode MOS transistors 282 and 284 are controlled by address signals, the McAdams reference clearly does not disclose an *isolation circuit* that disconnects *internal power supply bus* in response to a *control signal that indicates a standby mode.*

Accordingly, the McAdams reference fails to disclose all of the recited features of the instant claims, and thus, cannot possibly anticipate the claimed subject matter. As such, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claims 1-6 and 8-11.

Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 7 and 12 under 35. U.S.C. § 103(a) as being unpatentable over McAdams (U.S. Pat. No. 5,301,160) in view of Hoffman et al. (U.S. Pat. No. 5,117,129).

Applicants respectfully traverse this rejection. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of

the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

Claims 7 and 12 depend from independent claim 1 and are believed to be patentable based on this dependence, and further based on the additional subject matter separately recited in each of the claims. Applicants respectfully submit that the Hoffman reference does not cure the deficiencies of the McAdams reference. In the rejection, the Examiner admitted that the McAdams reference fails to disclose an isolation circuit coupled between a pad on the device configured to receive the power signal and the internal power supply bus, and an I/O pad and circuitry coupled between the output buffer and the I/O pad to tri-state the I/O pad, as recited in claims 7 and 12. The Examiner relied on the Hoffman reference, as disclosing these recited features. However, the Hoffman reference is directed to cold sparing of a full rail logic swing CMOS off-chip driver that presents high impedance to ground when power is not present. *See* Hoffman, col. 1, lines 36-39. Specifically, the reference describes a CMOS circuit that presents high impedance when the voltage V_{DD} is equal to ground. *See* Hoffman, col. 3, lines 1-5 and 37-56. In the Hoffman reference, the pad signal 150 is coupled to the I/O pad 152 through the circuit, which includes the transistor 158. *See* Hoffman, Fig. 3A, col. 3, lines 25-30. The circuit, which is coupled to the I/O pad 152, or even the transistor 158, which is coupled to other transistors 164, T1, T4, and T8, is not coupled to an *internal power supply bus,* as recited in the

present claims. Accordingly, the Hoffman reference does not disclose the subject matter recited in claims 7 and 12. Furthermore, the operation of the circuit is not based on a *control signal that indicates a standby-mode*, but based on the voltage V_{DD}. *See*, Hoffman, col. 3, lines 36-56. As such, the Hoffman reference does not disclose an *isolation circuit* that disconnects *internal power supply bus* in response to a *control signal that indicates a standby mode*. Therefore, claims 7 and 12 are patentable by virtue of their dependency from independent claim 1 as well as the subject matter recited in each of the claims. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of claims 7 and 12.

Conclusion

In view of the remarks and amendments set forth above, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of claims 1-12. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefore. Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MICS:0071/FLE (00-0901).

Respectfully submitted,

Date: 12/11/03

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